UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,921	03/24/2001	Bindiganavale S. Nataraj	NLM.P002	6229

27296 7590 02/09/2005

LAWRENCE M. CHO
P.O. BOX 2144
CHAMPAIGN, IL 61825

EXAMINER	
DAVIS, CYNTHIA L	
ART UNIT	**PAPER NUMBER**
2665	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/815,921	NATARAJ, BINDIGANAVALE S.	
	Examiner	Art Unit	
	Cynthia L Davis	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/24/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams in view of Srinivasan.

Regarding claim 1, a digital signal processor is disclosed in Williams, column 4, lines 46-47. A content addressable memory (CAM) array for storing entries is disclosed in column 4 of Williams, lines 45-46. A partitioned priority index table having a plurality of rows and columns of priority blocks, each row for storing a priority number associated with an entry in the CAM array is disclosed in column 6, line 45 (disclosing a connection table) and column 7, lines 43-48 (disclosing a priority field in the connection table). Each column having compare logic coupled to each of the priority blocks in its respective column, and an encoder coupled to the partitioned priority index table is missing from Williams. These are disclosed in Srinivasan at column 2, lines 31-32 (the comparators) and figure 1, element 30 (a priority encoder). It would have been obvious to one skilled in the art at the time of the invention to use the CAM of Srinivasan in the router of Williams (see Srinivasan, column 2, lines 14-19). The motivation would be to speed up the operation of the router.

Regarding claim 2, the encoder determines an index in the CAM array from among entries that match input data and have a most significant priority number is missing from Williams. However, Srinivasan discloses in column 4, lines 29-30, the priority encoder identifying the highest-priority data word that matches the search word. It would have been obvious to one skilled in the art at the time of the invention to use the CAM of Srinivasan in the router of Williams (see Srinivasan, column 2, lines 14-19). The motivation would be to speed up the operation of the router.

Regarding claim 3, the entries comprise policy statements and the priority numbers indicate the relative priority of policy statements is disclosed in column 7, lines 43-48 of Williams (the table may contain QoS information for each connection).

Regarding claim 4, the entries comprise Internet Protocol addresses and the priority numbers comprise prefix mask data for the Internet Protocol addresses is not specifically disclosed in Williams. However, Williams does disclose in column 6, line 45, that the table is a connection table, and in column 7, lines 43-47, that priority data may be stored. It would have been obvious to one skilled in the art at the time of the invention to use IP addresses and prefix mask data to identify the connections. The motivation would be to use an inherent quality of the connections to identify them.

2. Claims rejected under 35 U.S.C. 103(a) as being unpatentable over Williams in view of Srinivasan in further view of Lavi.

Regarding claim 5, the partitioned priority index table comprises a first row of priority blocks for storing a first plurality of priority numbers having bits in each of the priority blocks in the first row; a second row of priority blocks that stores a second

plurality of priority numbers having bits in each of the priority blocks in the second row; a first compare logic circuit that determines a most significant block priority number (MSBPN) for a first column of priority blocks from a first block priority number (BPN) from a first priority block in the first row and a BPN from a second priority block in the second row; and a second compare logic circuit that determines a MSBPN for a second column of priority blocks from a BPN from a third priority block in the first row and a BPN from a fourth priority block in the second row is missing from Williams. However, Williams does disclose in column 7, lines 43-48, priority fields in a CAM memory. Further, Lavi discloses in claim 7, in column 7, lines 33-38, a CAM memory arranged in rows and columns where the comparisons are done on a column by column basis. It would have been obvious to one skilled in the art at the time of the invention to do the comparisons on a column by column basis. The motivation would be to use an old technique in the CAM art.

Regarding claim 6, the first compare logic circuit comprises: a first stage comparator that compares the BPNs from the first and second priority blocks to determine the MSBPN for the first column; and a first second stage comparator that compares the MSBPN for the first column with the BPN from the first priority block to determine whether the MSBPN for the first column originated from the first priority block; and a second second stage comparator that compares the MSBPN for the first column with the BPN from the second priority block to determine whether the MSBPN for the first column originated from the second priority block is missing from Williams. However, Srinivasan discloses in column 2, lines 41-50, a system that determines the

most significant entry and the CAM cell in which that entry is stored. It would have been obvious to one skilled in the art at the time of the invention to use comparators to determine the most significant entry and its location. The motivation would be to locate the highest priority data in the CAM.

3. Claims 7, 15-18, 20, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavi in view of Williams.

Regarding claim 7, a first row of priority blocks for storing a first plurality of priority numbers having bits in each of the priority blocks in the first row; a second row of priority blocks that stores a second plurality of priority numbers having bits in each of the priority blocks in the second row; a first compare logic circuit that determines a most significant block priority number (MSBPN) for a first column of priority blocks from a first block priority number (BPN) from a first priority block in the first row and a BPN from a second priority block in the second row; and a second compare logic circuit that determines a MSBPN for a second column of priority blocks from a BPN from a third priority block in the first row and a BPN from a fourth priority block in the second row is disclosed in Lavi at claim 7, in column 7, lines 33-38 (disclosing a CAM memory arranged in rows and columns where the comparisons are done on a column by column basis). The data stored being priority numbers is missing from Lavi. However, Williams does disclose in column 7, lines 43-48, priority fields in a CAM memory. It would have been obvious to one skilled in the art at the time of the invention to store the priority information in a CAM in rows and columns. The motivation would be to have a convenient, widely-available sort of memory to use to store the priority information.

Regarding claim 15, the first compare logic circuit comprising a priority index table and the second compare logic circuit comprising a priority index table is missing from Lavi. However, Williams discloses in column 7, lines 43-48, priority indices in a CAM memory. It would have been obvious to one skilled in the art at the time of the invention to store the priority information in a CAM in rows and columns.

Regarding claim 16, a first compare logic circuit register that registers results from the first compare logic circuit for a second group of priority numbers while the second compare logic circuit determines the most significant block priority number for the second column for a first group of priority numbers are disclosed in Lavi, column 7, lines 38-45 (disclosing match lines that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM, and control bits that are set in response to the match lines).

Regarding claim 17, match line segments coupled to the third priority block; match line segments coupled to the fourth priority block; a first signal filtering circuit that de-asserts the match line segments coupled to the third priority block when the MSBPN for the first column does not originate from the first row; and a second signal filtering circuit that de-asserts the match line segments coupled to the fourth priority block when the MSBPN for the first column does not originate from the second row are disclosed in Lavi, column 7, lines 38-45 (disclosing match lines that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM, and control bits that are set in response to the match lines).

Regarding claim 18, the first and second signal filtering circuits comprise circuitry that performs an AND function is not specifically disclosed in Lavi. However, the AND function is well known in the art. It would have been obvious to one skilled in the art at the time of the invention to perform an AND function. The motivation would be to use a common type of logic function.

Regarding claim 20, match line segments coupled to the first signal filtering circuit; match line segments coupled to the second signal filtering circuit; a third signal filtering circuit that de-asserts the match line segments coupled to the first signal filtering circuit when the MSBPN for the second column does not originate from the first row; and a fourth signal filtering circuit that de-asserts the match line segments coupled to the second signal filtering circuit when the MSBPN for the second column does not originate from the second row are disclosed in Lavi, column 7, line 38-45 (disclosing match lines connected to all cells that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM).

Regarding claim 25, the priority numbers comprise prefix mask data for an Internet Protocol address is missing from Lavi. However, Williams does disclose in column 6, line 45, that the table is a connection table, and in column 7, lines 43-47, that priority data may be stored. It would have been obvious to one skilled in the art at the time of the invention to use IP addresses and prefix mask data to identify the connections. The motivation would be to use an inherent quality of the connections to identify them.

4. Claims 8-14, 19, and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavi in view of Williams in further view of Srinivasan.

Regarding claim 8, the first compare logic circuit comprising: a first stage comparator that compares the BPNS from the first and second priority blocks to determine the MSBPN for the first column; and a first second stage comparator that compares the MSBPN for the first column with the BPN from the first priority block to determine whether the MSBPN for the first column originated from the first priority block; and a second second stage comparator that compares the MSBPN for the first column with the BPN from the second priority block to determine whether the MSBPN for the first column originated from the second priority block is missing from Williams and Lavi. However, Srinivasan discloses in column 2, lines 41-50, a system that determines the most significant entry and the CAM cell in which that entry is stored. It would have been obvious to one skilled in the art at the time of the invention to use comparators to determine the most significant entry and its location. The motivation would be to locate the highest priority data in the CAM.

Regarding claim 9, match line segments coupled to the first priority block; match line segments coupled to the second priority block; a first signal filtering circuit that de-asserts the match line segments coupled to the first priority block when the MSBPN for the first column does not originate from the first row; and a second signal filtering circuit that de-asserts the match line segments coupled to the second priority block when the MSBPN for the first column does not originate from the second row are disclosed in Lavi, column 7, line 38-45 (disclosing match lines that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM).

Regarding claim 10, the first and second signal filtering circuits comprising circuitry that performs an AND function is not specifically disclosed in Lavi. However, the AND function is well known in the art. It would have been obvious to one skilled in the art at the time of the invention to perform an AND function. The motivation would be to use a common type of logic function.

Regarding claim 11, a first register coupled to the match line segments coupled to the first priority block and a second register coupled to the match line segments coupled to the second priority block that register match line segment results from the first and second priority blocks for a second group of priority numbers are disclosed in Lavi, column 7, lines 38-45 (disclosing match lines that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM, and control bits that are set in response to the match lines). The third and fourth priority blocks determining block priority numbers for a first group of priority numbers is

missing from Lavi. However, Srinivasan discloses in column 2, lines 41-50, a system that determines the most significant entry and the CAM cell in which that entry is stored. It would have been obvious to one skilled in the art at the time of the invention to determine more block priority numbers. The motivation would be to locate the highest priority data in the CAM.

Regarding claim 12, match line segments coupled to the third priority block; match line segments coupled to the fourth priority block; a third signal filtering circuit that de-asserts the match line segments coupled to the third priority block when the MSBPN for the second column does not originate from the first row; and a fourth signal filtering circuit that de-asserts the match line segments coupled to the fourth priority block when the MSBPN for the second column does not originate from the second row are disclosed in Lavi, column 7, line 38-45 (disclosing match lines connected to all cells that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM).

Regarding claim 13, a third compare logic circuit that determines a MSBPN for a third column of priority blocks from a BPN from a fifth priority block in the first row and a BPN from a sixth priority block in the second row is missing from Williams and Lavi. However, Srinivasan discloses in column 2, lines 41-50, a system that determines the most significant entry and the CAM cell in which that entry is stored. It would have been obvious to one skilled in the art at the time of the invention to use comparators to determine the most significant entry and its location. The motivation would be to locate the highest priority data in the CAM.

Regarding claim 14, match line segments coupled to the fifth priority block; match line segments coupled to the sixth priority block; a first signal filtering circuit that de-asserts the match line segments coupled to the fifth priority block when the MSBPN for the third column does not originate from the first row; and a second signal filtering circuit that de-asserts the match line segments coupled to the sixth priority block when the MSBPN for the third column does not originate from the second row are disclosed in Lavi, column 7, line 38-45 (disclosing match lines connected to all cells that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM).

Regarding claim 19, a first register coupled to the match line segments coupled to the first priority block and a second register coupled to the match line segments coupled to the second priority block that register match line segment results from the first and second priority blocks for a second group of a priority numbers are disclosed in Lavi, column 7, lines 38-45 (disclosing match lines that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM, and control bits that are set in response to the match lines). The third and fourth priority blocks determine block priority numbers for a first group of priority numbers is missing from Lavi. However, Srinivasan discloses in column 2, lines 41-50, a system that determines the most significant entry and the CAM cell in which that entry is stored. It would have been obvious to one skilled in the art at the time of the invention to determine more block priority numbers. The motivation would be to locate the highest priority data in the CAM.

Regarding claim 21, a third compare logic circuit that determines a MSBPN for a third column of priority blocks from a BPN from a fifth priority block in the first row and a BPN from a sixth priority block in the second row, where each of the BPNS from the fifth and sixth priority blocks is assigned the LSBPN if the MSBPN for the second column did not originate from its row is missing from Williams and Lavi. However, Srinivasan discloses in column 2, lines 41-50, a system that determines the most significant entry and the CAM cell in which that entry is stored. It would have been obvious to one skilled in the art at the time of the invention to use comparators to determine the most significant entry and its location. The motivation would be to locate the highest priority data in the CAM.

Regarding claim 22, match line segments coupled to the fifth priority block; match line segments coupled to the sixth priority block; a first signal filtering circuit that de-asserts the match line segments coupled to the fifth priority block when the MSBPN for the second column does not originate from the first row; and a second signal filtering circuit that de-asserts the match line segments coupled to the sixth priority block when the MSBPN for the second column does not originate from the second row are disclosed in Lavi, column 7, line 38-45 (disclosing match lines connected to all cells that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM).

Regarding claim 23, match line segments coupled to the first signal filtering circuit; match line segments coupled to the second signal filtering circuit; a third signal filtering circuit that de-asserts the match line segments coupled to the first signal filtering

circuit when the MSBPN for the third column does not originate from the first row; and a fourth signal filtering circuit that de-asserts the match line segments coupled to the second signal filtering circuit when the MSBPN for the third column does not originate from the second row.

Regarding claim 24, match line segments coupled to the fifth priority block; match line segments coupled to the sixth priority block; a first signal filtering circuit that de-asserts the match line segments coupled to the fifth priority block when the MSBPN for the third column does not originate from the first row; and a second signal filtering circuit that de-asserts the match line segments coupled to the sixth priority block when the MSBPN for the third column does not originate from the second row are disclosed in Lavi, column 7, line 38-45 (disclosing match lines connected to all cells that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM).

5. Claims 26-27, 30-32, and 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams in view of Lavi.

Regarding claim 26, a partitioned priority index table having a plurality of rows and columns of priority blocks is disclosed in Williams, column 6, line 45 (disclosing a connection table) and column 7, lines 43-48 (disclosing a priority field in the connection table). A first priority block in a first row that compares a first plurality of bits of a first plurality of priority numbers and determines a block priority number (BPN) for the first priority block; a second priority block in a second row that compares a first plurality of bits of a second plurality of priority numbers and determines a BPN for the second

priority block; a first compare logic circuit that determines a most significant block priority number (MSBPN) for a first column from the BPNs for the first and second priority blocks, a third priority block in the first row that compares a second plurality of bits of the first plurality of priority numbers and determines a BPN for the third priority block; a fourth priority block in the second row that compares a second plurality of bits of the second plurality of priority numbers and determines a BPN for the fourth priority block; and a second compare logic circuit that determines a MSBPN for the second column from the BPNS for the third and fourth priority block, where the BPNS for each of the third and fourth priority blocks are a least significant block priority number (LSBPN) if the MSBPN for the first column did not originate in its row is missing from Williams. However, Williams does disclose in column 7, lines 43-48, priority fields in a CAM memory. Further, Lavi discloses in claim 7, in column 7, lines 33-38, a CAM memory arranged in rows and columns where the comparisons are done on a column by column basis. It would have been obvious to one skilled in the art at the time of the invention to do the comparisons on a column by column basis. The motivation would be to use an old technique in the CAM art.

Regarding claim 27, match line segments coupled to the third priority block; match line segments coupled to the fourth priority block; a first signal filtering circuit that de-asserts the match line segments coupled to the third priority block when the MSBPN for the second column does not originate from the second row; and a second signal filtering circuit that de-asserts the match line segments coupled to the fourth priority block when the MSBPN for the second column does not originate from the second row

is missing from Williams. However, Lavi discloses in column 7, line 38-45, match lines connected to all cells that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM. It would have been obvious to one skilled in the art at the time of the invention to have match lines that are asserted or de-asserted based on a match in their row. The motivation would be to use an old technique in the CAM art.

Regarding claim 30, the first compare logic circuit comprises a priority index table and the second compare logic circuit comprises a priority index table are disclosed in Williams in column 7, lines 43-48 (priority indices in a table)

Regarding claim 31, match line segments coupled to the third priority block; match line segments coupled to the fourth priority block; a first signal filtering circuit that de-asserts the match line segments coupled to the third priority block when the MSBPN for the first column does not originate from the first row; and a second signal filtering circuit that de-asserts the match line segments coupled to the fourth priority block when the MSBPN for the first column does not originate from the second row is missing from Williams. However, Lavi discloses in column 7, line 38-45, match lines connected to all cells that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM. It would have been obvious to one skilled in the art at the time of the invention to have match lines that are asserted or de-asserted based on a match in their row. The motivation would be to use an old technique in the CAM art.

Regarding claim 32, the first and second plurality of priority numbers comprise prefix mask data for an Internet Protocol address is not specifically disclosed in Williams. However, Williams does disclose in column 6, line 45, that the table is a connection table, and in column 7, lines 43-47, that priority data may be stored. It would have been obvious to one skilled in the art at the time of the invention to use IP addresses and prefix mask data to identify the connections. The motivation would be to use an inherent quality of the connections to identify them.

Regarding claim 40, a partitioned priority index table, comprising a first row of priority blocks that stores a first plurality of priority numbers having bits in each of the priority blocks in the first row; a second row of priority blocks that stores a second plurality of priority numbers having bits in each of the priority blocks in the second row is disclosed in Williams, column 6, line 45 (disclosing a connection table) and column 7, lines 43-48 (disclosing a priority field in the connection table). Means for determining a most significant block priority number (MSPBN) from a first column of priority blocks from a first block priority number (BPN) from a first priority block in the first row and a BPN from a second priority block in the second row; and means for determining a MSBPN for a second column of priority blocks from a BPN from a third priority block in the first row and a BPN from a fourth priority block in the second row are not specifically discloses in Williams. However, Williams does disclose in column 7, lines 43-48, priority fields in a CAM memory. Further, Lavi discloses in claim 7, in column 7, lines 33-38, a CAM memory arranged in rows and columns where the comparisons are done on a column by column basis. It would have been obvious to one skilled in the art at the time

of the invention to do the comparisons on a column by column basis. The motivation would be to use an old technique in the CAM art.

Regarding claim 41, the means for determining the MSBPN for the first column comprising means for comparing the BPNS from the first and second priority blocks to determine the MSBPN for the first column; and means for comparing the MSBPN for the first column with the BPN from the first priority block to determine whether the MSBPN for the first column originated from the first priority block; and means for comparing the MSBPN for the first column with the BPN from the second priority block to determine whether the MSBPN for the first column originated from the second priority block is missing from Williams. However, Lavi discloses in claim 7, in column 7, lines 33-38, a CAM memory arranged in rows and columns where the comparisons are done on a column by column basis. It would have been obvious to one skilled in the art at the time of the invention to do the comparisons on a column by column basis. The motivation would be to use an old technique in the CAM art.

Regarding claim 42, means for de-asserting asserted match line segments from the first priority block when the MSBPN for the first column did not originate from the first row; and means for de-asserting asserted match line segments from the second priority block when the MSBPN for the first column did not originate from the second row is missing from Williams. However, Lavi discloses in column 7, lines 38-45, match lines that may be asserted or de-asserted based on the presence of a match in a specific column. It would have been obvious to one skilled in the art at the time of the

invention to assert or de-assert the match lines. The motivation would be to indicate the presence of important information in a particular place in the memory.

6. Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams in view of Lavi in further view of Srinivasan.

Regarding claim 28, a fifth priority block in the first row that compares a third plurality of bits of the first plurality of priority numbers and determines a BPN for the fifth priority block; a sixth priority block in the second row that compares a third plurality of bits of the second plurality of priority numbers and determines a BPN for the sixth priority block; and a third compare logic circuit that determines a MSBPN for the third column from the BPNS for the fifth and sixth priority block, where the BPNS for each of the fifth and sixth priority blocks are the LSBPN if the MSBPN for the second column did not originate in its row is missing from Williams and Lavi. However, Srinivasan discloses in column 2, lines 41-50, a system that determines the most significant entry and the CAM cell in which that entry is stored. It would have been obvious to one skilled in the art at the time of the invention to use comparators to determine the most significant entry and its location. The motivation would be to locate the highest priority data in the CAM.

Regarding claim 29, match line segments coupled to the fifth priority block; match line segments coupled to the sixth priority block; a first signal filtering circuit that de-asserts the match line segments coupled to the fifth priority block when the MSBPN for the third column does not originate from the first row; and a second signal filtering circuit that de-asserts the match line segments coupled to the sixth priority block when the

MSBPN for the third column does not originate from the second row is missing from Williams. However, Lavi discloses in column 7, line 38-45, match lines connected to all cells that may or may not be asserted depending on whether there is a match connected to each of the memory cells in the CAM. It would have been obvious to one skilled in the art at the time of the invention to have match lines that are asserted or de-asserted based on a match in their row. The motivation would be to use an old technique in the CAM art.

7. Claims 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan.

Regarding claim 33, Determining a first block priority number (BPN) from a first plurality of bits from a first plurality of priority numbers; determining a second BPN from a first plurality of bits from a second plurality of priority numbers, determining a most significant block priority number (MSBPN) for a first column from the first and second BPNs is not specifically disclosed in Srinivasan. However, Srinivasan discloses in column 2, lines 41-50, a system that selects the highest priority cell in a memory comprising an unspecified number of rows and columns. It would have been obvious to one skilled in the art at the time of the invention to determine a highest priority block in a column of a memory. The motivation would be to find the location of the most significant information in the memory.

Regarding claim 34, determining a third BPN from a second plurality of bits from the first plurality of priority numbers; determining a fourth BPN from a second plurality of bits from the second plurality of priority numbers; and determining a MSBPN for a

second column from the third and fourth BPNS, where the third BPN is assigned a least significant block priority number (LSBPN) if the MSBPN for the first column is not the first BPN, and the fourth BPN is assigned the LSBPN if the MSBPN for the first column is not the second BPN is not specifically disclosed in Srinivasan. However, Srinivasan discloses in column 2, lines 41-50, a system that selects the highest priority cell in a memory comprising an unspecified number of rows and columns. It would have been obvious to one skilled in the art at the time of the invention to determine a highest priority block in a column of a memory. The motivation would be to find the location of the most significant information in the memory.

Regarding claim 35, determining that a priority number associated with the third BPN is the most significant priority number for the device if the MSBPN for the second column is the third BPN; and determining that a priority number associated with the fourth BPN is the most significant priority number for the device if the MSBPN for the second column is the fourth BPN is not specifically disclosed in Srinivasan. However, Srinivasan discloses in column 2, lines 41-50, a system that selects the highest priority cell in a memory comprising an unspecified number of rows and columns. It would have been obvious to one skilled in the art at the time of the invention to determine a highest priority block in a column of a memory. The motivation would be to find the location of the most significant information in the memory.

Regarding claim 36, assigning the LSBPN being performed after determining the third BPN from the second plurality of bits from the first plurality of priority numbers and the fourth BPN from the second plurality of bits from the second plurality of priority

numbers is not specifically disclosed in Srinivasan. However, Srinivasan discloses in column 2, lines 41-50, a system that selects the highest priority cell in a memory comprising an unspecified number of rows and columns. It would have been obvious to one skilled in the art at the time of the invention to assign the LSBPN after determining the BPNs. The motivation would be to know the BPNs before attempting to decide which one of them was the most and least significant.

8. Claims 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan in view of Lavi.

Regarding claim 37, registering results from a determination of a fifth BPN from a first plurality of bits from a third plurality of priority numbers while determining the third BPN from the second plurality of bits from the first plurality of priority numbers; and registering results from a determination of a sixth BPN from a first plurality of bits from a fourth plurality of priority numbers while determining the fourth BPN from the second plurality of bits from the second plurality of priority numbers is missing from Srinivasan. However, Lavi discloses in column 7, lines 43-45, setting control bits in response to match signals from various columns in a memory. It would have been obvious to one skilled in the art at the time of the invention to register the results. The motivation would be to store the results for later use.

Regarding claim 38, determining a fifth BPN from a third plurality of bits from the first plurality of priority numbers; determining a sixth BPN from a third plurality of bits from the second plurality of priority numbers; and determining a MSBPN for a third column from the fifth and sixth BPN, where the fifth BPN is assigned the LSBPN if the

MSBPN for the second column is not the third BPN, and the sixth BPN is given the default LSBPN if the MSBPN for the second column is not the fourth BPN is not specifically disclosed in Srinivasan. However, Srinivasan discloses in column 2, lines 41-50, a system that selects the highest priority cell in a memory comprising an unspecified number of rows and columns. It would have been obvious to one skilled in the art at the time of the invention to determine a highest priority block in a column of a memory. The motivation would be to find the location of the most significant information in the memory.

Regarding claim 39, determining that a priority number associated with the fifth BPN is the most significant priority number for the device if the MSBPN for the third column is the fifth BPN; and determining that a priority number associated with the sixth BPN is the most significant priority number for the device if the MSBPN for the third column is the sixth BPN is not specifically disclosed in Srinivasan. However, Srinivasan discloses in column 2, lines 41-50, a system that selects the highest priority cell in a memory comprising an unspecified number of rows and columns. It would have been obvious to one skilled in the art at the time of the invention to determine a highest priority block in a column of a memory. The motivation would be to find the location of the most significant information in the memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia L Davis whose telephone number is (571) 272-3117. The examiner can normally be reached on 8:30 to 6, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLD
1/17/2005

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600